Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-42 (Canceled)

Claim 43 (Previously presented): A tested semiconductor device comprising electrical contact terminals and scrub marks on ones of the electrical contact terminals produced by a process comprising:

providing a wafer having a plurality of semiconductor devices thereon, each of said semiconductor devices including a plurality of electrical contact terminals;

adjusting a planar orientation of probe elements of a probe card assembly to correspond to a planar orientation of said electrical contact terminals by changing a planar orientation of a probe substrate to which said probe elements are attached with respect to a probe card of said probe card assembly, a complaint electrical connection flexing to maintain electrical connections between electrical contacts on said probe card of said probe card assembly and said probe substrate,

effecting contact between ones of said electrical contact terminals of ones of said semiconductor devices and ones of said probe elements, said contact causing said ones of said probe elements to be pressed with a contact force against and to wipe across said ones of said contact terminals of said ones of said semiconductor devices and thereby make scrub marks on at least a plurality of said terminals of a first of said ones of said semiconductor devices ~~said ones of said contact terminals~~; and

testing said ones of said semiconductor devices,

wherein said first of said ones of said semiconductor devices is said tested semiconductor device.

Claims 44-47 (Canceled)

Claim 48 (Previously presented): The tested semiconductor device of claim 43, wherein the process further comprises dicing said wafer to singulate said semiconductor devices.

Claim 49 (Previously presented): The tested semiconductor device of claim 43, wherein said probe substrate comprises a space transformer.

Claim 50 (Canceled)

Claim 51 (Previously presented): The tested semiconductor device of claim 102, wherein said moveable element comprises a threaded element.

Claim 52 (Previously presented): The tested semiconductor device of claim 102, wherein said moveable element comprises a screw.

Claim 53 (Previously presented): The tested semiconductor device of claim 52, wherein said screw comprises a differential screw.

Claim 54 (Previously presented): The tested semiconductor device of claim 102, wherein moving said moveable element in a first direction causes at least a portion of said probe substrate to move toward said probe card.

Claim 55 (Previously presented): The tested semiconductor device of claim 54, wherein moving said moveable element in a second direction allows at least a portion of said probe substrate to move away from said probe card.

Claim 56 (Previously presented): The tested semiconductor device of claim 102, wherein said moveable element comprises a servo mechanism disposed to alter a position of said probe substrate with respect to said probe card.

Claim 57 (Previously presented): The tested semiconductor device of claim 102, wherein said moveable element comprises a piezoelectric actuator disposed to alter a position of said probe substrate with respect to said probe card.

Claim 58 (Canceled)

Claim 59 (Previously presented): The tested semiconductor device of claim 43, wherein said probe elements are elongate and resilient.

Claim 60 (Currently amended): The tested semiconductor device of claim 102, wherein said moveable element is capable of planarizing tips of said probe elements with respect to said electrical contact terminals ~~of said semiconductor device~~.

Claim 61 (Previously presented): The tested semiconductor device of claim 102, wherein said moveable element comprises a pivot structure.

Claim 62 (Previously presented): The tested semiconductor device of claim 61, wherein said pivot structure is disposed against said probe substrate.

Claim 63 (Previously presented): The tested semiconductor claim 102, wherein said moveable element comprises a sphere.

Claim 64 (Previously presented): The tested semiconductor device of claim 102, wherein said moveable element comprises a differential screw that comprises an outer threaded portion and an inner threaded portion.

Claim 65 (Previously presented): The tested semiconductor device of claim 102, wherein said probe substrate is mounted to said probe card by a means that is different than said moveable element.

Claims 66-73 (Canceled)

Claim 74 (Previously presented): The tested semiconductor device of claim 102 wherein:
said probe substrate is mounted to said probe card with a biasing force, and
said moveable element is configured to apply a force in opposition to said biasing force.

Claim 75 (Previously presented): The tested semiconductor device of claim 99, wherein:

said interposer comprises a substrate and a plurality of conductive vias passing through said substrate, and

one elongate interconnection element in each of said pairs of elongate interconnection elements is electrically connected to one end of one of said vias and said other elongate interconnection element in each of said pairs of elongate interconnection elements is electrically connected to an opposite end of said one of said vias.

Claim 76 (Previously presented): The tested semiconductor device of claim 75, wherein:

said interposer further comprises a plurality of first terminals disposed on a first side of said interposer and a plurality of second terminals disposed on a second side of said interposer,

ones of said vias electrically connect ones of said first terminals with ones of said second terminals, and

said one elongate interconnection element in each of said pairs of elongate interconnection elements is attached to one of said first terminals and said other elongate interconnection element in each of said pairs of elongate interconnection elements is attached to one of said second terminals.

Claim 77 (Previously presented): The tested semiconductor device of claim 99, further comprising a plurality of conductive passages through said probe substrate, and wherein:

ones of said probe elements are electrically connected to one end of ones of said conductive passages,

one elongate interconnection element in each of said pairs of elongate interconnection elements is in electrical contact with an opposite end of said ones of said conductive passages, and

said other elongate interconnection element in each of said pairs of elongate interconnection elements is in electrical contact with one of said electrical contacts of said probe card.

Claim 78 (Previously presented): The tested semiconductor device of claim 97 further comprising fastening means for moveably fastening said probe substrate to said probe card, wherein said interposer floatingly engages said probe card and said probe substrate without being fastened to said probe substrate or said probe card.

Claim 79 (Previously presented): The tested semiconductor device of claim 99, wherein only tips of said elongate interconnection elements of said interposer touch said probe card or said probe substrate.

Claim 80 (Previously presented): The tested semiconductor device of claim 43, wherein said effecting contact comprises bringing said ones of said probe elements into contact with said ones of said electrical contact terminals of said ones of said semiconductor devices.

Claim 81 (Previously presented): The tested semiconductor device of claim 102, wherein said moveable element is capable of altering a planar orientation of said probe substrate with respect to a planar orientation of said probe card.

Claims 82-92 (Canceled)

Claim 93 (Previously presented): The tested semiconductor device of claim 102, wherein said adjusting further comprises adjusting a planarity of said probe elements of said probe substrate by moving said moveable element.

Claim 94 (Previously presented): The tested semiconductor device of claim 93, wherein said adjusting further comprises adjusting said planarity of said probe elements of said probe substrate with respect to an expected planarity of said electrical contact terminals of said ones of said semiconductor devices.

Claim 95 (Previously presented): The tested semiconductor device of claim 93, wherein said adjusting further comprises leveling said probe elements with respect to an expected planarity of said electrical contact terminals of said ones of said semiconductor devices.

Claim 96 (Previously presented): The tested semiconductor device of claim 102, wherein each said probe element comprises a spring, whereby said probe elements provide individual compliance with respect to said contact terminals of said semiconductor devices and said moveable element provides global planarization of said probe elements with respect to said contact terminals.

Claim 97 (Previously presented): The tested semiconductor device of claim 43, wherein said compliant electrical connection comprises an interposer disposed between said probe card and said probe substrate.

Claim 98 (Previously presented): The tested semiconductor device of claim 97, wherein said electrical connections between said probe card and said probe substrate pass through said interposer.

Claim 99 (Previously presented): The tested semiconductor device of claim 97, wherein said interposer comprises a plurality of paired elongate interconnection elements extending from opposite sides of said interposer, said paired interconnection elements providing said electrical connections between said probe card and said probe substrate.

Claim 100 (Previously presented): The tested semiconductor device of claim 43, wherein said compliant electrical connection comprises springs configured to exert a first force against said probe card and a second force against said probe substrate.

Claim 101 (Previously presented): The tested semiconductor device of claim 100, wherein said springs of said compliant electrical connection are electrically conductive and provide said electrical connections between said probe card and said probe substrate.

Claim 102 (Previously presented): The tested semiconductor device of claim 43, wherein said adjusting a planar orientation comprises moving a moveable element disposed to alter an orientation of said probe substrate with respect to said probe card.

Claim 103 (Previously presented): The tested semiconductor device of claim 43 further comprising providing said probe card assembly, wherein providing said probe card assembly comprises fabricating said probe elements to have contact tips disposed in a generally uniform plane, said contact tips configured to contact said terminals of said semiconductor devices.

Claim 104 (Previously presented): The tested semiconductor device of claim 103, wherein said fabricating said probe elements comprises:

planarizing probe bodies; and

attaching said contact tips to said probe bodies.

Claim 105 (Previously presented): The tested semiconductor device of claim 103, wherein said fabricating said probe elements comprises:

attaching probe bodies to said probe substrate;

planarizing said probe bodies with respect to a surface of said probe substrate; and

attaching said contact tips to said probe bodies.

Claim 106 (Previously presented): The tested semiconductor device of claim 105, wherein said attaching probe bodies to said probe substrate comprises attaching wire stems to said probe substrate.

Claim 107 (Previously presented): The tested semiconductor device of claim 106, wherein said planarizing said probe bodies comprises:

encapsulating said wire stems in material; and

planarizing said material and said wire stems.

Claim 108 (Currently amended): The tested semiconductor device of claim 43, wherein the scrub marks are substantially uniform <u>across said plurality of said terminals of said first of said ones of said semiconductor devices</u>.

Claim 109 (Previously presented): The tested semiconductor device of claim 108, wherein the scrub marks are substantially uniform in accordance with the adjusted planarity.

Claim 110 (New): The tested semiconductor device of claim 43, wherein said adjusting a planar orientation is performed while said probe card assembly is mounted to a wafer tester comprising a chuck for holding said wafer.

Claim 111 (New): The tested semiconductor device of claim 43, wherein:

said process further comprises mounting said probe card assembly to a wafer tester, and placing said wafer on a chuck of said wafer tester;

said effecting contact comprises moving said chuck such that said ones of said electrical contact terminals of said ones of said semiconductor devices of said wafer are brought into contact with said ones of said probe elements of said probe card assembly; and

said adjusting a planar orientation further comprises:

prior to placing said wafer on said chuck, placing a test plate on said chuck;

bringing said test plate into contact with said probe elements;

determining whether said probe elements substantially simultaneously contact said test plate; and

if said probe elements do not substantially simultaneously contact said test plate, changing said planar orientation of said probe substrate with respect to said probe card, and repeating said bringing and said determining until determining that said probe elements substantially simultaneously contact said test plate.